

Claims

1. An integrated circuit comprising;  
a semiconductor substrate;  
5 an optical waveguide formed over the substrate;  
an insulating planarization layer formed adjacent  
the optical waveguide and level with the top of the  
waveguide; and  
a microwave transmission line formed over the  
10 planarization layer and overlying a top surface of the  
optical waveguide.
2. A circuit as claimed in claim 1, wherein the  
insulating planarization layer comprises a tetra-ethyl-  
15 ortho-silicate (TEOS) layer.
3. A circuit as claimed in claim 1, wherein the  
semiconductor substrate comprises a compound  
semiconductor.  
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4. A circuit as claimed in claim 3, wherein the  
semiconductor is Gallium Arsenide-based.
5. A circuit as claimed in claim 1, wherein the optical  
25 waveguide comprise a multiple layer structure, in which a  
substantially undoped Gallium Arsenide layer is  
sandwiched between substantially undoped Aluminium  
Gallium Arsenide layers.
- 30 6. A circuit as claimed in claim 1 comprising an  
electro-optic modulator, wherein two optical waveguide  
sections are formed over the substrate, and wherein a  
respective transmission line for each waveguide section  
is formed over the planarization layer.

7. A circuit as claimed in claim 6, wherein the waveguide sections are parallel and spaced apart, the spacing between the waveguide sections being filled with  
5 the planarization layer.

8. A circuit as claimed in claim 6, wherein the waveguide sections are parallel and spaced apart, an air gap being provided in the spacing between the waveguide  
10 sections.

9. A circuit as claimed in claim 8, wherein semiconductor portions are provided adjacent the waveguide sections for supporting the transmission lines.

15 10. A circuit as claimed in claim 6, wherein a common conduction layer is provided beneath the waveguide sections.

20 11. A circuit as claimed in claim 6, wherein the insulating planarization layer comprises a tetra-ethyl-ortho-silicate (TEOS) layer.

25 12. A circuit as claimed in claim 6, wherein the semiconductor is Gallium Arsenide-based.

13. A method of fabricating an integrated circuit comprising;

providing a semiconductor substrate;

30 depositing multiple semiconductor layers over the substrate;

patterning the multiple layers to define an optical waveguide stack formed over the substrate, the multiple

layers being removed from the lateral sides of the waveguide stack;

depositing a planarization layer to fill the sides of the waveguide stack with a planarization layer to the 5 same height as the waveguide stack; and

forming a microwave transmission line over the planarization layer and contacting a top surface of the optical waveguide stack.

10 14. A method as claimed in claim 13, wherein the insulating planarization layer comprises a tetra-ethyl-ortho-silicate (TEOS) layer.

15 15. A method as claimed in claim 13, wherein the semiconductor is Gallium Arsenide-based.

20 16. A method as claimed in claim 13, wherein the multiple semiconductor layers comprise a substantially undoped Gallium Arsenide layer sandwiched between substantially undoped Aluminium Gallium Arsenide layers.

25 17. A method as claimed in claim 13 for fabricating an electro-optic modulator, wherein the patterning of the multiple layers defines two optical waveguide stacks, and wherein a respective transmission line for each waveguide stack is formed over the planarization layer.

30 18. A method as claimed in claim 17, wherein the waveguide stacks are parallel and spaced apart, and wherein the spacing between the waveguide sections is filled with the planarization layer.

19. A method as claimed in claim 17, the planarization layer is not formed between the waveguide stacks.

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20. A method as claimed in claim 17, wherein the patterning of the multiple layers further defines bridge portions adjacent the waveguide stacks.

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